9 nm to 135 nm, which are to prevent the spread of depletion layers from being constrained at the interface between the crystallized semiconductor layer and the underlevel protection layer.

2. (Amended) A thin film semiconductor device, comprising:

a substrate;

an underlevel protection layer including an insulating material, the underlevel protection layer being formed on at least a portion of the substrate; and

a field effect transistor having:

a semiconductor film on the underlevel protection layer;

a gate insulator layer formed on the semiconductor film,

a gate electrode formed on the gate insulator layer; and

an electrically insulating interlevel insulator layer formed over the gate electrode and between interconnects of said field effect transistor, the underlevel protection layer, the gate insulator layer, and the interlevel insulator layer comprising a silicon oxide film and having a combined thickness of about 2 μm or less.

REMARKS

Claims 1 and 2 are pending. By this Amendment, claims 1 and 2 are amended. Reconsideration based on the above amendments and the following remarks is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten claim (37 C.F.R. §1.121(c)(1)(ii)).

I. Claim 2 Satisfies the Requirements Under 35 U.S.C. §112, first paragraph

Claim 2 is rejected under 35 U.S.C. §112, first paragraph, as containing subject matter not sufficiently described in the specification. Claim 2 is now amended and obviates the rejection.